AC Bias-Temperature Stability of a-InGaZnO Thin-Film Transistors With Metal Source/Drain Recessed Electrodes

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***Abstract*— In this paper, we fabricated metal source/drain recessed nearly self-aligned amorphous indium–gallium–zinc–oxide thin-film transistors (TFTs) that are highly stable under ac bias-temperature stress (BTS). For TFTs of the size $W/L = 60\ \mu$m/10 μm, the stress-induced threshold voltage shifts are all within −0.35 V. A comprehensive investigation of ac BTS stress polarity, frame time, and duty cycle dependence is presented in the context of high-resolution high-refresh rate active-matrix flat-panel displays. We find that higher frequency bipolar ac pulses increase the device instability. The threshold voltage instability may be reduced significantly by decreasing the duty cycle of the stress waveform.**

***Index Terms*— AC, active-matrix flat-panel display (AM-FPD), amorphous indium–gallium–zinc–oxide (a-IGZO), bias-temperature stress (BTS), electrical stability, self-aligned, thin-film transistor (TFT).**

I. Introduction

THE amorphous indium–gallium–zinc–oxide (a-IGZO) thin-film transistor (TFT) is a promising candidate as the backplane technology for next-generation active matrix liquid crystal displays [1], active-matrix light-emitting diode (AM-OLED) [2], and low-power mobile displays [3]. Its notable advantages include: high field-effect mobility (μ_{FE}), low off-state leakage current (I_{OFF}), transparency in visible light spectrum, low-temperature deposition, and uniform amorphous deposition over a large substrate area [4]–[7].

The threshold voltage (V_{th}) stability of TFTs under current-temperature stress (CTS) and bias-temperature stress (BTS) are critical factors for robust displays with long lifetime. Stable devices are desirable so as to avoid the complex pixel circuit designs that would be required to compensate for significant V_{th} degradation (ΔV_{th}) [8]. Under constant CTS conditions for which TFTs are subjected to in an AM-OLED display, a-IGZO TFTs are found to be much more reliable ($\Delta V_{th} = 0.2$ V) than a-Si:H TFTs ($\Delta V_{th} > 1.8$ V) [9]. Steady-state (dc) positive and negative BTS, both in the dark and illuminated, have been the subject of much theoretical and experimental research effort and are well documented [10]–[13]. Our group previously reported that the dc BTS-induced ΔV_{th} instability of a-IGZO TFTs is significantly lower than that of a-Si:H TFTs [14], in agreement with the experimental data in the published literature.

Although there is substantial work on the dc BTS stability of a-IGZO TFTs, the steady-state condition is not an accurate representation of active-matrix flat panel display (AM-FPD) operation, which biases the transistors in positive and negative alternating (ac) pulses. A direct comparison of ac and dc BTS on a-Si:H TFTs shows that dc BTS reliability is a poor predictor of ac BTS ΔV_{th} [15]. Thus, there is strong motivation to study and verify ac BTS behavior such that the lifetime of a-IGZO TFT backplane technology may be properly evaluated.

For the ac BTS of a-IGZO TFTs, only a small number of studies have been published. Existing literatures are all limited in the scope of stress conditions and are often performed on devices with poor electrical properties and/or reliability. Fung *et al.* [16] investigated the pulsewidth (PW) dependence of ΔV_{th} in a-IGZO TFTs with an inverted-staggered bottom-gate structure. They reported a strong PW dependence for positive unipolar ac BTS, with larger ΔV_{th} for longer PWs up to 100 ms. Negative unipolar ac BTS exhibited very small ΔV_{th} and no obvious trend regarding PW was observed. Ohta *et al.* [11] showed that after 100 h of stressing, ac BTS-induced ΔV_{th} for a-IGZO TFT is about half that of a-Si:H TFT. In terms of stress conditions, the effect of different duty cycles [17] and pulse rise times [18] have also been studied for different device structures. However, these devices showed $|\Delta V_{th}| > 5$ V after less than 10^4 s of stressing, suggesting that the observed ΔV_{th} may be the result of other fabrication deficiencies and not truly characteristic of a-IGZO. A swing back of the ΔV_{th} toward its initial state (i.e., recovery) or the opposite polarity has been observed for both positive unipolar [19] and bipolar ac BTS [20], but not negative unipolar pulses. Furthermore, existing data on the PW dependence of the positive unipolar ac BTS are inconsistent for different structures/processes, where some showed increased instability for dc and longer PWs (more dc-like) [16], [19] while others are the opposite (greater ΔV_{th} for shorter PWs, positive steady state is the smallest) [18], [21].

Finally, ac BTS produces observable change in the TFT capacitance–voltage measurement after stressing [20], similar to dc BTS [10].

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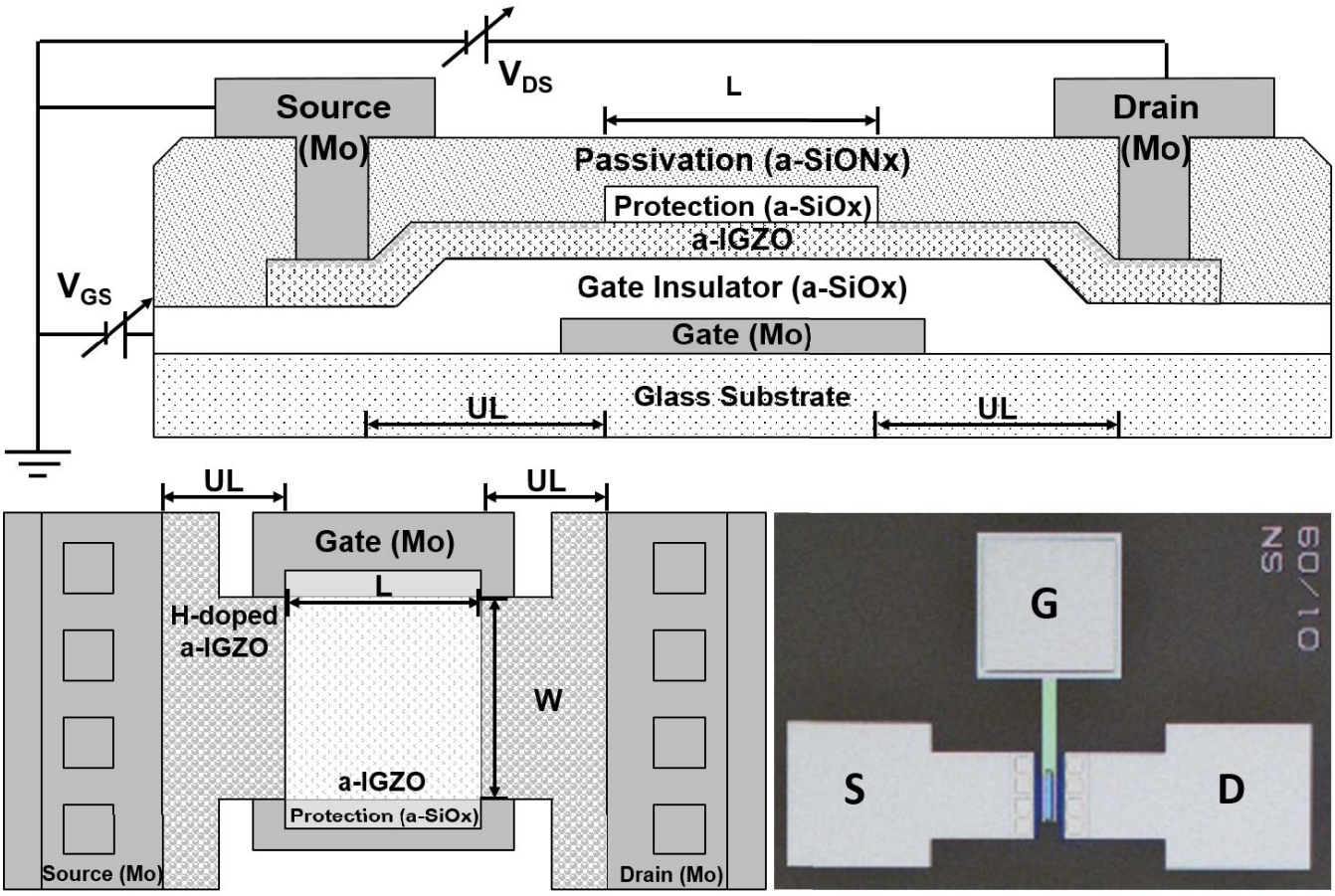

Fig. 1. (Top) cross-sectional and (lower left) top-view diagram of the a-IGZO TFT used throughout this paper. (Lower right) top-view micrograph of the fabricated device.

Our objective in this paper is to fabricate highly reliable bottom-gate a-IGZO TFTs with reduced gate to source/drain (S/D) capacitance (C_{GS}) and evaluate their electrical stability under ac BTS. We present a comprehensive set of data on ac electrical stability using a broad set of stress conditions: polarity, frame time (1/frequency), and duty cycle. Our devices are all very stable under ac BTS and the $|\Delta V_{th}|$ for all stress conditions are within 0.35 V or less after 10^4 s of stressing at temperature of $T_{st} = 70$ °C in ambient air.

II. Experiment

The molybdenum gate electrode (100 nm) is first deposited on the glass substrate by sputtering, then patterned, and defined by dry etching using CF_4/O_2 plasma. The gate insulator is a layer of amorphous silicon oxide (a-SiO_x) (200 nm) deposited with plasma-enhanced chemical vapor deposition (PECVD) at 340 °C. The a-IGZO active layer (40 nm) is dc sputtered and defined (islands) using dilute hydrochloric acid. The a-SiO_x channel protection layer (CPL) (300 nm) is deposited by PECVD at 285 °C and dry etched to define device geometry. After CPL definition, the substrate is treated in a rapid thermal anneal oven at 290 °C for 1 h. The amorphous silicon oxynitride (a-$SiON_x$) passivation layer (300 nm) is then deposited by PECVD at 250 °C, during which the hydrogen in the PECVD process chamber and/or the hydrogen-rich a-$SiON_x$ layer dopes the a-IGZO regions not covered by the CPL. This process greatly reduces the resistivity of a-IGZO [22], thus creating nearly self-aligned H-doped S/D contact regions. The a-IGZO area defined by the CPL width (W) and length (L) are considered the device dimensions, and in this paper, the TFTs studied have $W/L = 60\ \mu$m/10 μm. The S/D contact via is opened in the passivation layer by dry etching. Molybdenum S/D electrodes (100 nm) are then sputtered and wet etched using a dilute phosphoric and nitric acid mixture. In this TFT configuration, the Mo S/D electrode edges are recessed with respect to the Mo gate electrode edges. There is a separation/underlap (UL) of about 20 μm between the CPL and the S/D via. Such device structure is expected to produce significantly lower S/D-gate parasitic capacitance (C_{GS}) in comparison with other TFT structures described in the literature. After processing, the TFTs undergo one more anneal at 270 °C in ambient atmosphere for 1 h. The top-view diagram, cross-sectional diagram, and top-view micrograph of the complete device are shown in Fig. 1.

It should be indicated that if back exposure is used in combination with the gate electrode as mask, the top CPL can be fully self aligned to the gate dimensions. In addition, the CPL is used as mask for H-doping, hence creating the nearly self-aligned H-doped S/D regions. Such device structure is

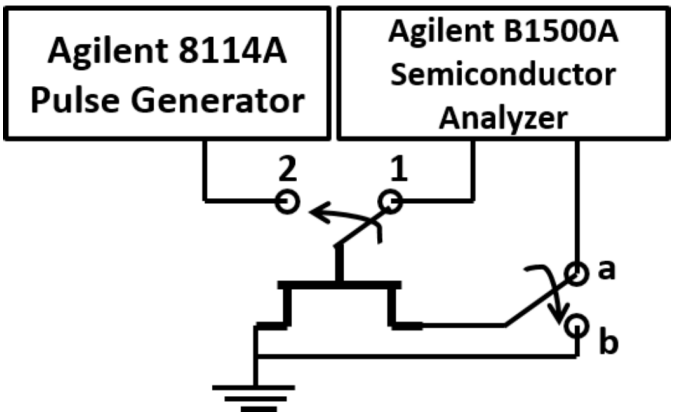

Fig. 2. Diagram showing the experimental setup switching between stressing (switch positions 1, a) and characterization (switch positions 2, b) steps by the E5250A switching matrix.

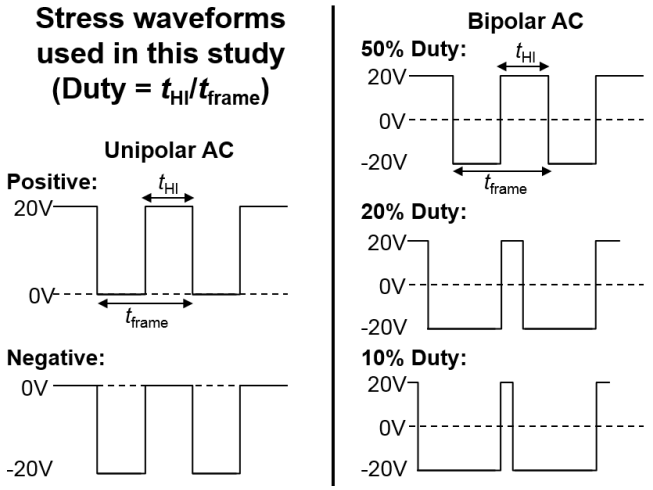

Fig. 3. Different gate bias stress waveforms used in this paper. (Left) Unipolar positive and negative pulses. (Right) Bipolar pulses of different duty cycles.

expected to have a reduced overlap between the S/D regions and gate electrode; as shown in Fig. 1, the S/D metal electrodes do not overlap at all with the gate metal electrode (reversed TFT structure). In this TFT structure, we still maintain small overlap between H-doped a-IGZO regions and gate electrode. We expect that this overlap will not affect C_{GS}. Both these effects will be responsible for significant reduction of C_{GS} in comparison with other TFT structures used in previous BTS investigations. Therefore, this BTS study is novel and significant because it can be applied to future high-resolution flat panel displays.

Throughout this paper, device measurement and stressing are done at $T_{st} = 70$ °C on a heated chuck in the dark; the illumination effect is not addressed in this paper. The a-IGZO TFT transfer characteristics (I_D–V_{GS}) in the linear ($V_{DS} = 0.1$ V) and saturation ($V_{DS} = 15$ V) regions between $V_{GS} = -10$ and 10 V are measured at 0.1 V steps using an Agilent B1500A semiconductor analyzer. The TFT source electrode is always grounded during device measurement.

The B1500A and a HP 8114A pulse generator are connected to an HP E5250A switching matrix. An Agilent EasyExpert software routine is responsible for switching the E5250A between the 8114A for ac stressing and the B1500A for device measurement and dc stressing, as shown in Fig. 2. During stressing, the source and drain electrodes are tied together and grounded ($V_{DS} = 0$ V) to ensure a uniform distribution of the electric field across the channel. The device stressing is interrupted at predetermined time intervals to measure the TFT transfer characteristics at $T_{st} = 70$ °C. This repeats until total accumulated stress time reaches 10^4 s. Total accumulated stress time is defined as the amount of time a nonzero gate bias (positive or negative) is applied to the gate. A different TFT on the same wafer is used for each stress condition.

For ac gate stress, the three types of waveforms used in this paper are shown in Fig. 3: positive unipolar ($V_{G-Stress} = 0$ to $+20$ V), negative unipolar (0 to -20 V), and bipolar (-20 to $+20$ V). The duty cycle of a stress waveform is defined as the ratio of positive PW to frame time (t_{HI}/t_{frame}), and frame time is the inverse of frequency. For unipolar ac waveforms, the duty cycle is fixed at 50%, so t_{HI} is always one half the frame time. For bipolar ac waveforms, the duty cycle is varied from 10% to 50%. In the case of unipolar ac stressing, because the gate bias is 0 V for half the frame time, the stress waveform needs to be applied for double the duration (i.e., 2×10^4 s) to achieve the same accumulated stress time (10^4 s) as dc or bipolar ac stressing.

III. Experimental Results and Discussion

The device transfer characteristics before stress are shown in Fig. 4(a). The TFT field-effect mobility in the linear region is extracted by fitting the linear region transfer curve in Fig. 4(a) [23]. The threshold voltage is extracted by extrapolating the x-intercept of the fit. The TFT used in this paper has the parameters $\mu_{FE} = 10.9$ cm^2/V· s and $V_{th} = -1.03$ V. We also extracted the subthreshold swing (SS) of the TFT, for which the $\partial \log I_D/\partial V_{GS}$ is taken as the average of three values nearest the maximum slope point in the subthreshold region of the transfer curve. The SS of TFT studied is calculated to be 220 mV/decade. From the device transfer characteristics, we observe that I_{OFF} is in the order of 10^{-14} A at room temperature (not shown). The drain current is independent of the gate and drain voltage in the off-region. The off-current actually increases to the order of 10^{-12} A when measured at 70 °C, and it should be noted that this is actually a result of increased thermal noise in the measurement setup at an elevated temperature. Table I summarizes the extracted device parameters of the a-IGZO TFT at 70 °C. An example of the TFT transfer characteristics after undergoing ac BTS is shown in Fig. 4(b) and appears almost identical to that of the unstressed device. In fact, all TFTs stressed show no visible changes in μ_{FE}, SS, and I_{OFF} under any of the ac BTS stress schemes applied throughout this paper, with the only noticeable degradation being ΔV_{th}.

For the a-Si:H TFT, it has been shown in a side-by-side comparison that a combination of positive and negative dc BTS cannot accurately predict ac BTS stability. In this paper, we apply a similar methodology [15] to the a-IGZO TFT. The threshold voltage instability ΔV_{th} for a particular stress time t_{st} is defined as $\Delta V_{th}(t = t_{st}) = V_{th}(t = t_{st})V_{th}(t = 0)$. In Fig. 5, ΔV_{th} over accumulated stress time for the positive and

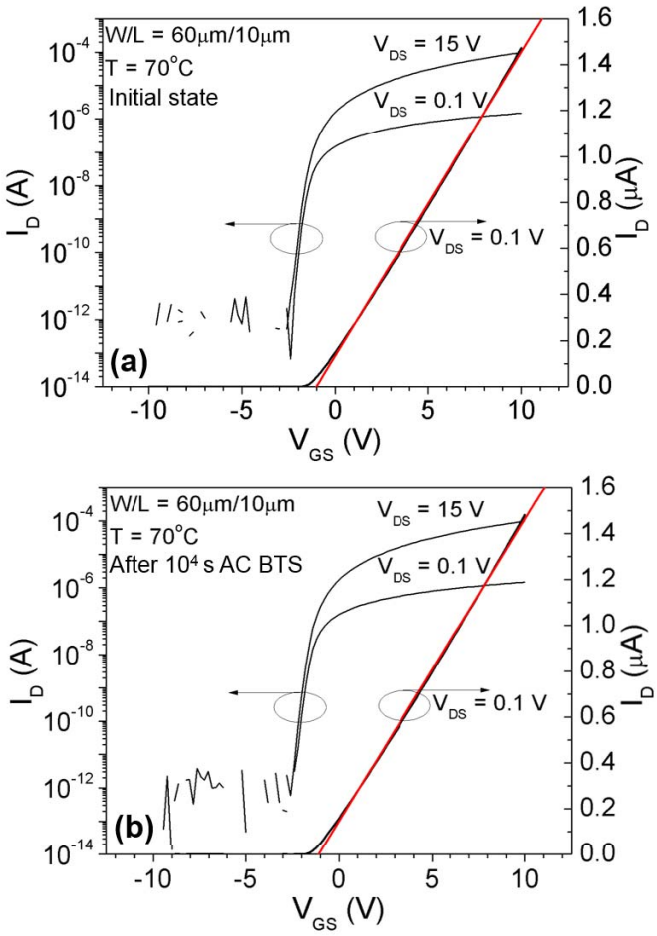

Fig. 4. Transfer characteristics in the linear region (V_{DS} = 0.1 V) and saturation region (V_{DS} = 15 V) of (a) a-IGZO TFT used in this paper and (b) same TFT after receiving 10^4 s of ac BTS. (Red line) The linear fit of the device ID at the 20% and 80% points.

TABLE I
EXTRACTED DEVICE PARAMETERS OF THE a-IGZO TFTs IN THE LINEAR REGION

μ_{EF} [cm²/V·s]	V_{th} [V]	SS [mV/dec]	I_{OFF} [A]
10.9	-1.03	220	$<10^{-12}$

negative dc BTS, their sum, and bipolar ac BTS (PW = 10 ms) are shown superimposed in the same figure. It is clear that the sum of steady-state behavior significantly overestimates the ac BTS instability of a-IGZO TFTs. In Fig. 6, we compare the sum of positive and negative unipolar ac BTS with bipolar ac BTS of equal frame time and stress voltage magnitude. We consider the positive and negative unipolar ac waveforms as two halves from which the bipolar waveform can be constructed from. This relationship is described by $\Delta V_{th}^{\pm} = \Delta V_{th}^{+} + \Delta V_{th}^{-}$. In this figure, we observe that the curve of the sum very closely follows that of the bipolar ac BTS instability. From this, we can conclude that to model or predict the lifetime of AM-FPD with a-IGZO TFT backplane technology, ac BTS evaluation is required.

In Fig. 7, we investigate the effect of frame time dependence for both (a) positive (+20 V) and (b) negative (−20 V) unipolar ac BTS instability as a function of accumulated stress

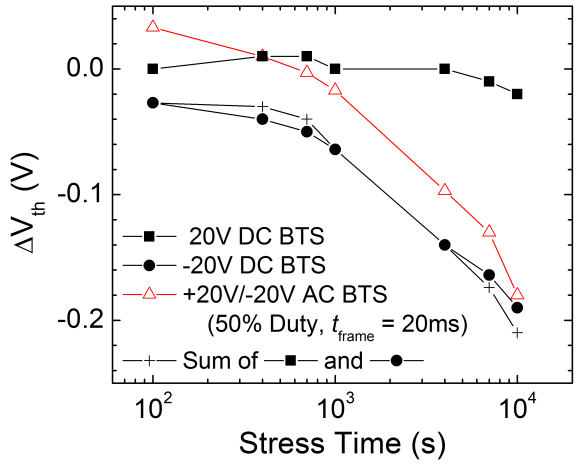

Fig. 5. Side-by-side comparison of bipolar ac BTS (open triangles) and the sum (crosshair marks) of positive (solid squares) and negative (solid circles) dc BTS. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

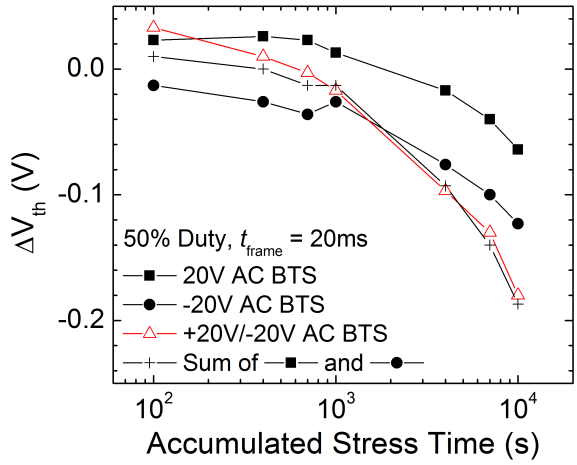

Fig. 6. Side-by-side comparison of bipolar ac BTS (open triangles) and the sum (crosshair marks) of positive (solid squares) and negative (solid circles) unipolar ac BTS. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

time. For positive unipolar pulses, the ΔV_{th} of the devices are all negative and very insignificant (within −0.1 V), therefore no clear conclusion can be drawn regarding the frame time dependence for positive unipolar ac stressing. However, upon closer examination, we find that the ΔV_{th} values actually are positive within the first 1000 s of BTS, beyond which they trend negative until the end of the duration tested. For negative gate biases, the ΔV_{th} are all invariably negative and the magnitudes increase with accumulated stress time. In this case, the frame time dependence is much more obvious and larger t_{frame} cause greater ΔV_{th} instability. Regarding the strong dependence of negative unipolar ac BTS ΔV_{th} on frame time, we can consider the dc case to be the upper limit and calculate the $\Delta V_{th}^{AC}/\Delta V_{th}^{DC}$ as a function of frame time, which is shown in Fig. 8.

One notable advantage of the a-IGZO TFT is that its superior electron mobility compared with a-Si:H TFT will enable next-generation ultrahigh refresh rate displays (240–480 Hz) [24]. In Fig. 9, we evaluate the ac BTS stability of a-IGZO TFTs with bipolar waveforms mimicking AM-FPD

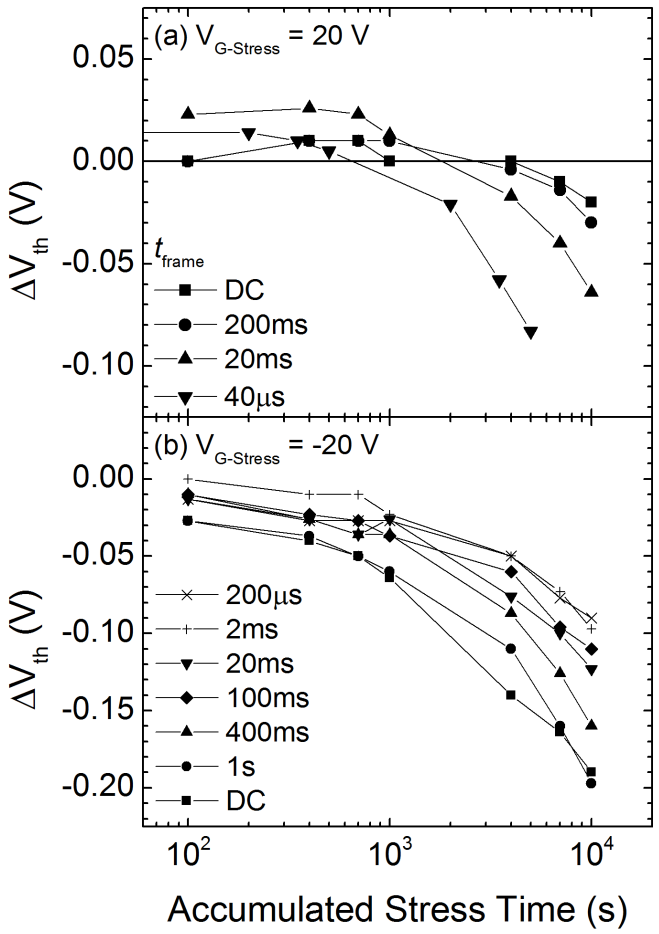

Fig. 7. Frame time dependence of the a-IGZO TFT threshold voltage instability under (a) positive unipolar ac BTS and (b) negative unipolar ac BTS. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

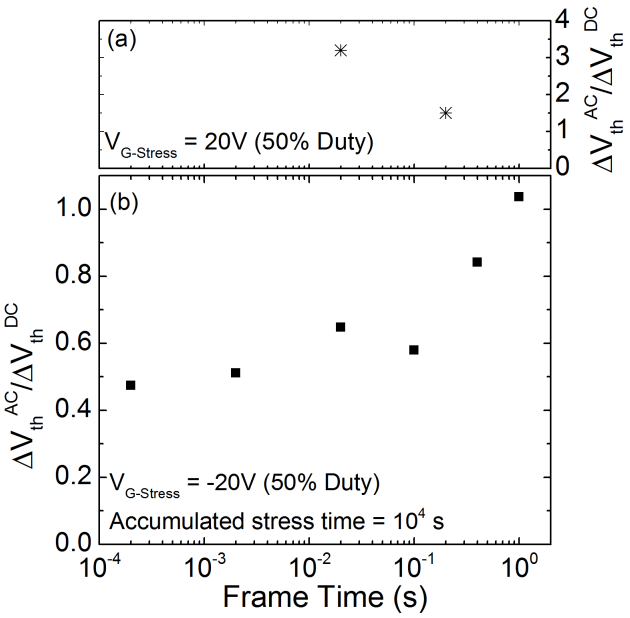

Fig. 8. AC BTS-induced threshold voltage shift as a function of ac stress frame times, normalized to the (a) positive or (b) negative dc BTS shift. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

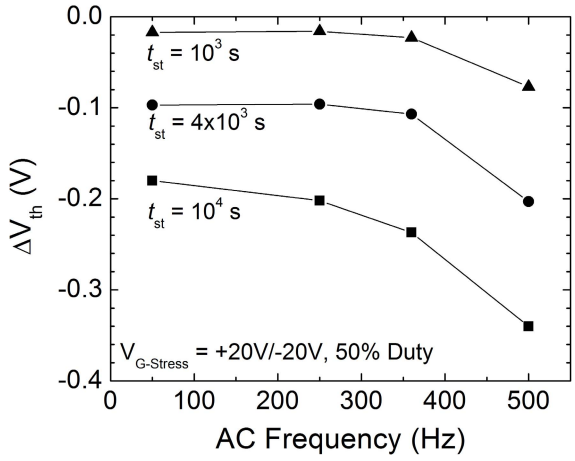

Fig. 9. AC BTS-induced threshold voltage shift as a function of applied bipolar stress frequency ($1/t_{frame}$). The duty cycle is kept at 50% for all frequencies. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

pixel addressing under higher frame rates. The duty cycles of the waveforms are fixed at 50%, which for bipolar pulses mean that higher frequency is equivalent to shorter frame time. From the figure, we observe that for $t_{st} = 1000$ s (solid triangle symbols), frequencies 360 Hz and below cause almost no ΔV_{th} while it becomes slightly more noticeable at 500 Hz. After $t_{st} = 10^4$ s, this effect is magnified such that the ΔV_{th} induced by the 500-Hz waveform is almost 150% that of the ΔV_{th} induced by the 360-Hz waveform. We observe higher ΔV_{th} with higher operation frequency, up to −0.35 V for 500 Hz, and this should be taken into consideration when using a-IGZO TFTs for ultrahigh refresh rate AM-FPDs.

We then investigate for the bipolar ac BTS the effect of varying the duty cycle of the stress waveforms. Referring to Fig. 3, we fix the frame time t_{frame} at 20 ms (50 Hz), while applying gate stress pulses with duty cycle values of 10%, 20%, and 50%. These duty cycle values would represent positive gate bias of +20 V being applied for 2, 4, and 10 ms within each frame, respectively, while −20 V is applied for the rest of the frame. In Fig. 10, we observe that when compared with 50% duty cycle, ΔV_{th} trends smaller for lower duty cycle values. This is better shown in Fig. 11, where we plot ΔV_{th} with respect to duty cycle for three different t_{st} values. We that see for all t_{st}, the ΔV_{th} is always smaller for lower duty cycle, and this effect is even more pronounced for longer t_{st}. Considering that higher frequency operation causes more instability in a-IGZO TFTs, adjusting the duty cycle and reducing the time portion of the positive bias segments (t_{HI}) may help reduce ΔV_{th} significantly. However, doing so may have an impact on the a-IGZO TFT pixel circuit design. In the dynamic response of an a-IGZO one-capacitor one-transistor test circuit, it is desirable to minimize the error voltage or the level-shift voltage (ΔV_P), which can be achieved by increasing the storage capacitance (C_{ST}) [25] or reducing C_{GS} value. It has been shown that larger C_{ST} also causes the charging time (t_{CH}) to increase, for which we are limited by the duty cycle and t_{HI} of the transistor driving waveform. This is expected to become an important factor to consider in the design of a-IGZO TFT pixel circuits for 8 K × 4 K and long lifetime AM-FPDs.

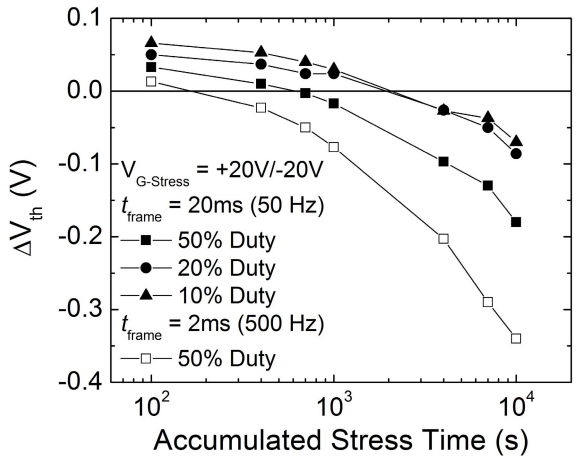

Fig. 10. AC BTS-induced threshold voltage shift as a function of accumulated stress time for different bipolar stress pulse duty cycles (10%, 20%, and 50%) at $t_{\text{frame}} = 20$ ms (50 Hz). The ΔV_{th} induced by ac stress with $t_{\text{frame}} = 2$ ms (500 Hz) is reproduced here for reference. Stressing and measurements are done at $T_{\text{st}} = 70$ °C in ambient air in the dark.

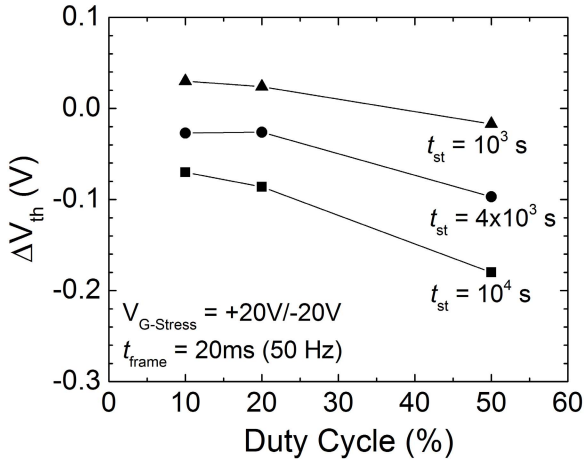

Fig. 11. AC BTS-induced threshold voltage shift as a function of duty cycle at $t_{\text{frame}} = 20$ ms (50 Hz) for different accumulated stress times. Stressing and measurements are done at $T_{\text{st}} = 70$ °C in ambient air in the dark.

In general, during our ac BTS, we observe ΔV_{th} shifting toward more negative values under both negative and positive BTS, i.e., V_{th} becomes more negative. What is the microscopic origin of such threshold voltage shift? This is a very important question thus far nobody was able to address or even speculate about. Most of the publications indicate that BTS produces some kind of defects within the bandgap without providing any discussion about their microscopic origin or energy location. We can only speculate that under PBTS and NBTS, there is formation of positively charged sites located near the gate insulator/a-IGZO interface, since we can only observe V_{th} shift without any change of SS or μ_{FE} during ac BTS; most likely, these sites are located within the gate oxide layer. Let us assume that PECVD silicon oxide gate insulator layer has a certain density of Si-based traps located at energy within the bandgap of a-IGZO that can emit electrons under certain bias conditions. Under PBTS, the electrons associated with such traps will be attracted toward the gate electrode, leaving positively charged sites (Si^+) near the interface that can produce negative V_{th} as experimentally observed. Under NBTS, the electrons are attracted toward a-IGZO, leaving behind again positively charged (Si^+) sites located near the gate oxide/a-IGZO interface. This will create negative ΔV_{th} as observed. More experiments will be needed to prove or disprove this suggestion.

IV. Conclusion

We have fabricated high-performance and highly stable bottom-gate S/D recessed nearly self-aligned a-IGZO TFTs that have a-$SiON_x$ as passivation layer. A comprehensive ac BTS study is conducted on a-IGZO TFTs, and they have been demonstrated to be very reliable under a wide variety of stressing conditions at 70 °C. We find that for our TFTs, the bipolar ac BTS instability time evolution can be well described by a simple sum of the positive and negative unipolar ac BTS instability, but not the sum of the dc BTS instabilities. The ac frame time dependence of the threshold voltage shift is thoroughly investigated. We find that negative unipolar pulses exhibit larger (more negative) ΔV_{th} shift for longer frame times. For positive unipolar pulses, the ΔV_{th} are initially positive and eventually trend toward negative for all frame time.

For bipolar ac BTS, we find that instability also has a dependence on the operation frequency and that higher frequency causes more instability. This is an important issue that should be addressed for high-refresh rate flat-panel displays. Upon changing the duty cycle of bipolar pulses from 50% to 10%, we can suppress the ΔV_{th} for the same operation frequency. This shows that different pixel addressing schemes, in the form of duty cycle control, may be viable for improving device stability.

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